University of Toledo
Electrical Engineering Technology
Master Syllabus

Course Title: Digital Systems Design **Course Code & Number: EET 3350**

Credit Hour Total: 4 Semester Hours

Lecture Contact Hours: 3 **Lab Contact Hours: 2**

Pre-requisite: EET 3150, UNIX, C, and Internet

Text: Digital Design Essentials, Richard Sandige, Prentice Hall Publishers.

Software: Xilinx ISE 6.1, Model Sim (VHDL), Mentor Graphics

A. Course Description

This course covers the design, analysis and applications of digital systems involving sequential circuits. Special attention is given to the formal analysis and design procedures for synchronous sequential logic circuits and bi-stable memory devices. Design projects focus on top-down design methodology using CAD tools and VHDL hardware description language.

B. Related Program Outcomes (a, b, c, d, e, f, g, k):

- An understanding of the analytical and laboratory skills associated with electrical engineering technology **(outcome a)**, as evidenced by the ability to perform:
  - Analysis of complex digital circuits using the concepts of characteristic equations, present state-next state tables, flow maps, transition maps, state diagrams, state reduction tables, and timing analysis.
  - Design and analysis using VHDL hardware description language and Xilinx CAD tools in a computer laboratory to model, simulate, and analyze complex digital circuits.
- An ability to apply current knowledge and adapt to emerging applications of mathematics, science and technology **(outcome b)**, as evidenced by the ability:
  - To review, digest, and apply the latest design techniques in the area of digital circuits by studying various conference and journal papers.
- An ability to conduct, analyze, and interpret experiments concerning digital circuits, as evidenced by **(outcome c)**:
  - The ability to perform various lab exercises using VHDL and Xilinx Software.
  - Written reports for select experiments.

- An ability to use creativity in the design and use of digital systems and processes as evidenced by **(outcome d)**:
    - The ability to design novel digital circuits using commercial CAD tools.
    - The ability to solve open ended problems .
- An ability to function as part of a team, as evidenced by **(outcome e)**:
    - Working with other students in a team of 3 to 4 students on a project.
- An ability to identify, analyze and solve technical problems associated with digital systems design , as evidence by **(outcome f)**:
    - An ability to solve problems on class quizzes, tests, and final examination.
    - An ability to participate in class discussions and solve problems open for discussion during class time.
- An ability to communicate effectively, as evidenced by **(outcome g)**:
    - Oral presentation of project work.
    - Written reports of projects.
- A commitment to quality and continuous improvement as evidenced by **(outcome k)**:
    - The ability to produce high quality project reports.
    - The ability to use the latest state of the art technology and digital CAD tools.
    - The ability to learn from past mistakes made on quizzes and tests and perform better in future, as evidenced by improvement in test scores, etc.

C. Course Objectives:

- To use digital CAD tools including VHDL and Xilinx ISE Software. Ability to design, simulate and test digital circuits using CAD tools. Students are required to submit written lab reports for appropriate lab experiments.
- To design and analyze combinational and sequential digital circuits using systematic design procedures.
- To design and innovate digital circuits for practical applications using Circuit delay models, Characteristic equations, PS/NS tables, State diagrams, and Boolean algebra.
- To work as part of a team. All students are required to do a team project for this course. Students will be required to submit a written report as well as give an oral presentation.
- To read journal/conference papers and other scientific magazines (IEEE Spectrum and IEEE Computer, etc.) and to keep abreast of the latest technological developments in the area of digital circuits.

D. Course Outline – Major Content Areas

- Programmable logic devices (PAL, PLA, PROM).
- Basic bi-stable memory devices.
- Analysis tools including: circuit delay models, characteristic equations, PS/NS tables, state diagrams, Karnaugh maps, transition maps, flow-maps, and timing diagrams.
- Additional bi-stable memory devices including various types of gated, master-slave, and edge-triggered flip-flops.
- Moore, Mealy, and mixed type synchronous machines including synchronous design procedure, designing with edge-triggered devices, and synchronous analysis procedure.
- Synchronous sequential design of Moore and Mealy machines including timing diagram description, state reduction by implication table, and state assignments.
- Synchronous counter design including shift-register counters, ring counters, and twisted ring counter design.
- Field Programmable Gate Arrays (FPGAs)
- VHDL Hardware Description Language.

E. Major Laboratory Topics

- Behavioral VHDL Design, Simulation, and Verification of Digital Circuits using ModelSim.
- Structural VHDL Design, Simulation, and Verification of Digital Circuits using ModelSim.
- Design of Half and Full Adders Using VHDL.
- Design of Flip Flops using VHDL.
- Design of Mixed Circuits using VHDL.
- Design of Shift Registers and Counters using State Cad Tools from Xilinx.
- Design of Traffic Light Controller Using CAD Tools.

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